

## ABSTRACT OF THE DISCLOSURE

2           An eye diagram analyzer equips each SUT data and clock signal input channel with individually  
variable delays in their respective paths. For a range of signal delay of  $n$ -many SUT clock cycles, the SUT  
4   clock signal delay might be set at about  $n/2$ . For each data channel there is specified a point in time  
relative to an instance of the delayed clock signal (data signal delay) and a voltage threshold. The  
6   specified combination (data signal delay, threshold and which channel) is a location on an eye diagram,  
although the trace may or may not ever go through that location. A counter counts the number of SUT  
8   clock cycles used as instances of the reference for the eye diagram, and another counter counts the  
number of times the specified combination of conditions was met ("hits"). After watching a specified  
10   combination for the requisite length of time or number of events, the number of SUT clock cycles  
involved and the associated number of hits are stored in memory using a data structure indexed by the  
12   components of the specified combination (data signal delay, threshold). Next, a new combination of data  
signal delay and threshold is specified and a measurement taken and recorded in the data structure. The  
14   process is repeated until all possible combinations within a stated range of data signal delay and threshold  
voltage (using specified resolution/step sizes for delay and voltage) have been investigated. As this  
16   process proceeds under the control of firmware within the logic analyzer, other firmware can be  
examining the data structure and generating a partial eye diagram visible on a display, and that will be  
18   complete soon after the measurement itself is finished.